REMARKS

Amendments

Claims 1-38 are pending. Claims 1-8, 12-23, 25, 28, 35, 37-38 are amended to clarify what is claimed and to specify that the iterating initialization cycle is an iterating process that iterates at least twice and performs a power up initialization cycle of the memory device during each iteration. The form of this language was agreed upon in the Examiner Interview of September 14, 2005, a summary of which is included herewith. Applicant reserves the right to reintroduce the original subject matter in one or more continuing applications.

Claim Rejections Under 35 U.S.C. § 102

The Advisory Action maintains the rejections of the Final Office Action.

Specifically, the Advisory Action of September 1, 2005 and the Final Office Action of June 16, 2005 rejected claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 under 35 U.S.C. § 102(a) as being anticipated by applicants' admitted prior art (the AAPA). Applicant respectfully traverses this rejection and submits that claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 are allowable for at least the following reasons.

In the Examiner Interview of September 14, 2005, Applicant and the Examiner discussed the pending claims and computer systems and memory device power-up initialization.

Applicant and the Examiner discussed that as power is first applied to computer systems during power-up it is generally not initially stable and at full voltage. This fluctuation in supply power can prevent the proper power-up initialization of the processors and other devices incorporated in the system, preventing proper operation and possibly corrupting data, as stated in Paragraph [0009] of the Specification of the Present Application. As such, most devices are designed to wait until power has stabilized before starting their power-up initialization and subsequent operation. In processors, this is usually accomplished by a power/reset watchdog circuit that asserts reset and holds the device in a reset condition until power has stabilized. Memory devices typically also have to go through a power-up initialization process or cycle before they can be available for access by the memory controller or processor of a system. The fluctuation as power is first applied to the system can corrupt the initialization process of the

memory devices incorporated in the system, preventing proper initialization and possibly corrupting data and/or preventing access to them. This initialization in one example of a Flash memory device of the prior art can take as much as 50us to 100us to complete. (*See,* Paragraph [0010] of the Specification of the Present Application).

Prior art memory devices typically either risk initialization failure by power-up initializing immediately or waiting to begin power-up initialization until they are commanded/signaled to initialize by the operating system memory controller or processor after power is stable, the processor/controller must then wait to access the memory device until the memory's initialization process completes (50us to 100us). In one synchronous Flash memory device of the prior art this power-up initialization signaling is accomplished by the RP# signal line. Unfortunately not all SDRAM compatible memory controllers have or utilize the RP# signal pin. (*See,* Paragraph [0010] of the Specification of the Present Application). Memory devices of the present invention begin to execute their power-up initialization process immediately upon receiving power and continue to continuously repeat the initialization process or cycle until told to stop by the system memory controller or processor. This allows memory embodiments of the present invention to be immediately available for access after receiving the stop command or signal and to avoid issues with power-up initialization corruption because at least one initialization cycle (the final full initialization cycle to run) will have completed while the power is stable. (*See,* Paragraphs [0034]-[0036] of the Specification of the Present Application). Memory device embodiments of the present invention can also be utilized in systems that do not have/cannot utilize the RP# signal line.

Applicant and the Examiner also discussed that SDRAM's and their commands are specified in standards promulgated by the JEDEC (Joint Electron Device Engineering Council) standards organization and that an external command referred to a signal such as an electronic signal on a hardware signal line, a system signal, or a software command or sequence sent to the memory device to stop the repeating initialization process of an embodiment of the present invention.

As requested by the Examiner, Applicant has included courtesy copies of U.S. Patent No. 6,178,501, titled "Method and apparatus for initializing a memory device", issued January 23, 2001, and U.S. Patent No. 6,675,255, titled "Device initialize command for a synchronous

memory", issued January 6, 2004 as references to corroborate the Applicant's statements regarding computer systems and memory devices. Applicant in particular notes Column 2, Lines 38-67 of U.S. Patent No. 6,178,501 and Column 14, Lines 27-61 of U.S. Patent No. 6,675,255.

The Examiner indicated in the Examiner Interview of September 14, 2005 that claims 1-38 may be allowable if they were amended to specifically claim an initialization cycle that repeated two or more times and incorporated an external electronic signal or SDRAM STOP command to stop power-up initialization, but that another search was required. As stated above, the Applicant has amended the claims as discussed with the Examiner in the Examiner Interview.

As noted in the Response to Final filed on August 16, 2005, the claims recite limitations to iterating, continuously looping, and repeating initialization cycles that repeat two or more times. The Office Action and Advisory Action has not identified any admission or prior art reference corresponding to such iterating, continuously looping or repeating initialization cycles. A device that initiates an initialization in response to a control signal and executes that initialization once to completion cannot read on Applicant's claim as it is neither iterating, continuously looping or repeating as required in Applicant's claims. Thus, the Office Action and Advisory Action fails to identify a reference teaching each and every limitation of Applicant's claims. On this basis alone, Applicant continues to contend that a rejection under 35 U.S.C. § 102(a) cannot be maintained.

In rejecting claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36, the Examiner stated that "[a] synchronous flash memory interface is disclosed in paragraph 7. The synchronous flash memory device beginning initialization upon receiving a power signal (RP#) on a power bus (signals are inherently delivered on a bus) is disclosed in paragraph 28 and in prior art figure 2. Stopping the initialization in response to an external command is inherent in the prior art figure 2 – a computer must be told what to do. Therefore an "external command" must be issued to stop the initialization."

Applicant respectfully maintains, that even if the Examiner is correct in his assertions of Applicant's Admissions of Prior Art, which the Applicant disputes, the synchronous Flash memory disclosed in Paragraphs [0007], [0028], and Figure 2 does not teach or disclose all elements of the Applicant's claimed invention. Applicant maintains that Paragraphs [0007],

[0028] and Figure 2 of the Present Application teach a synchronous Flash memory that starts its initialization cycle only upon receiving an external command, in the form of a RP# signal or a LCR command which is asserted by an external controller after power is up and stabilized, and then completes its initialization 50μS - 100μS later without receiving an external command that terminates the cycle. Applicant therefore submits that Paragraphs [0007], [0028] and Figure 2 of the Present Application do not teach a synchronous Flash memory that starts its initialization cycle upon receiving a power signal and iteratively, continuously or repeatedly executes this initialization cycle until it is terminated by an external command, as claimed by the Applicant.

Applicant's claim 1, as amended, recites, in part, "wherein the synchronous Flash memory device begins an iterating process upon receiving a power signal on a power bus, and stops the iterating process upon receiving an external electronic command, and where the iterating process iterates at least twice and performs an initialization cycle of the synchronous Flash memory device during each iteration." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a synchronous Flash memory device. As such, the AAPA fails to teach or disclose all elements of independent claim 1.

Applicant's claim 8, as amended, recites, in part, "wherein the memory device commences a continuously looping cycle upon receiving a power signal, and stops the continuously looping cycle upon receiving an external system signal, and where the continuously looping cycle loops at least twice and performs an initialization of the memory device during each loop." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a memory device. As such, the AAPA fails to teach or disclose all elements of independent claim 8.

Applicant's claim 17, as amended, recites "[a] method of initializing a synchronous Flash memory device comprising commencing a continuously looping cycle upon receiving a power signal, where the continuously looping cycle loops at least twice and performs a power up initialization of the synchronous Flash memory device during each loop; and stopping the continuously looping cycle upon receiving an external system command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 17.

Applicant's claim 22, as amended, recites "[a] method of initializing a memory device comprising starting a repeating initialization cycle upon receiving a power signal on a power

distribution line, wherein the repeating initialization cycle repeats at least twice and performs a power up initialization of the memory device during each repetition; and stopping the repeating initialization cycle upon receiving an external system command." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a method. As such, the AAPA fails to teach or disclose all elements of independent claim 22.

Applicant's claim 28, as amended, recites, in part, a system having a synchronous Flash memory device "wherein the synchronous Flash memory device begins an iterating process upon receiving a power signal on a power bus, and stops the iterating process upon receiving an external system command, where the iterating process iterates at least twice and performs a power up initialization cycle of the memory device during each iteration." As detailed above, Applicant submits that the AAPA fails to teach or disclose such a system having a synchronous Flash memory device that begins an iterating initialization cycle upon receiving a power signal on a power bus, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose all elements of independent claim 28.

Applicant respectfully contends that claims 1, 17, 22 and 28 have been shown to be patentably distinct from the cited reference. As claims 4-10, 12-14, 18-20, 23-27, 29-31 and 33-36 depend from and further define claims 1, 17, 22 and 28, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(a) and allowance of claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36.

The Advisory Action of September 1, 2005 and the Final Office Action of June 16, 2005 also rejected claims 37-38 under 35 U.S.C. § 102(e) as being anticipated by Kessler (U.S. Patent No. 6,820,196). Applicant respectfully traverses this rejection and reserves the right to swear behind the cited reference. The Applicant submits that claims 37-38 are allowable for at least the following reasons.

As noted above with respect to the rejections under 35 U.S.C. § 102(a), a device that initiates an initialization in response to a control signal and executes that initialization once to completion is not iterative as required in Applicant's claims 37 and 38. Thus, the cited reference

fails to teach each and every limitation of Applicant's claims. On this basis alone, Applicant contends that a rejection under 35 U.S.C. § 102(e) cannot be maintained.

Applicant continues to maintain that Kessler teaches a television set-top-box (STB) that checks the contents of and selectively initializes the data contents of an internal Flash memory device upon power up. Applicant has carefully reviewed the reference and has not found reference in Kessler to the internal device initialization that the Flash memory device must perform before it can make itself available on the data bus for read and write access by the processor, as maintained by the Examiner. Applicant respectfully maintains that the cited Figures 1 and 3 of Kessler refer to the system (the STB) powering up, checking the protected/formatted status of the Flash memory, and initializing the Flash memory data contents if the device is not formatted. (*See, e.g.*, Kessler, Abstract, Figures 1 and 3, Column 1, lines 48-63, and Column 3, lines 10-29). Applicant therefore respectfully submits that Kessler does not teach or disclose a synchronous Flash memory that begins to iterate an initialization cycle upon receiving Vcc and stops the initialization cycle in response to an external command.

Applicant's claim 37, as amended, recites, in part, a computer system that has "a memory device coupled to the host controller, wherein the memory device begins to iterate a repeating initialization cycle in response to Vcc, and stops iterating the initialization cycle in response to the host controller, wherein the initialization cycle repeats at least twice and performs a power up initialization of the memory device during each iteration." As detailed above, Applicant submits that Kessler fails to teach or disclose such a memory device that begins iterating a repeating initialization cycle in response to Vcc, and stops iterating the initialization cycle in response to the host controller. As such, Kessler fails to teach or disclose all elements of independent claim 37.

Applicant's claim 38, as amended, recites a method of operating a computer system "starting an iterating process in the memory device, wherein the iterating process iterates at least twice and performs a power up initialization cycle of the memory device during each iteration; and stopping iteration of the iterating initialization cycle process in the memory device in response to a software command from the host controller." As detailed above, Applicant submits that Kessler fails to teach or disclose such a method. As such, Kessler fails to teach or disclose all elements of independent claim 38.

Applicant respectfully contends that claims 37-38 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 37-38.

Claim Rejections Under 35 U.S.C. § 103

The Advisory Action of September 1, 2005 and the Final Office Action of June 16, 2005 rejected claims 2-3, 11, 21, and 15-16 under 35 U.S.C. § 103(a) as being anticipated over applicants' admitted prior art in view of SGS-THOMSON ST 10F 166. Applicant respectfully traverses this rejection and feels that claims 2-3, 11, 21, and 15-16 are allowable for the following reasons.

Applicant continues to respectfully note that, as stated above in regards to the rejection of independent claims 1, 8 and 17 from which claims 2-3, 11 and 21 depend, the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose independent claims 1, 8 and 17 and therefore does not teach or suggest all elements of claims 2-3, 11 and 21. In addition, Applicant respectfully maintains that cited reference ST10F166 discloses a microcontroller with an internal 256k Flash memory and thus submits that ST10F166 also does not teach disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. Therefore combining the elements of the AAPA with cited reference ST10F166 does not teach or suggest all elements of claims 1, 8 and 17. The Applicant therefore maintains that claims 1, 8 and 17 are thus allowable over the AAPA and cited reference ST10F166, either alone or in combination. As claims 2-3, 11 and 21 depend from and further define claims 1, 8 and 17, claims 2-3, 11 and 21 are also deemed allowable.

In regards to independent claims 15 and 16, the Applicant respectfully submits that, as stated above, the AAPA fails to teach or disclose such a memory device that begins an iterating cycle upon receiving a power signal, and stops the iterating cycle upon receiving an external command, where the iterating cycle iterates two or more times and performs a power up initialization of the synchronous Flash memory device during each iteration. As such, the AAPA

fails to teach or suggest all elements of claims 15 and 16. In addition, cited reference ST10F166 also does not teach disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. Therefore combining the elements of the AAPA with the cited reference ST10F166 does not teach or suggest all elements of claims 15 and 16. The Applicant therefore maintains that claims 15 and 16 are thus allowable over the AAPA and cited reference ST10F166, either alone or in combination.

Applicant respectfully contends that claims 2-3, 11, 21, and 15-16 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 2-3, 11, 21, and 15-16.

The Advisory Action of September 1, 2005 and the Final Office Action of June 16, 2005 also rejected claim 32 under 35 U.S.C. § 103(a) as being unpatentable over applicants' admitted prior art. Applicant respectfully traverses this rejection and feels that claim 32 is allowable for the following reasons.

Applicant respectfully notes that, as stated above in regards to the rejection of independent claim 28 from which claim 32 depends, the AAPA fails to teach or disclose such a memory device that begins an iterating initialization cycle upon receiving a power signal, and stops the iterating initialization cycle upon receiving an external command. As such, the AAPA fails to teach or disclose independent claim 28 and therefore does not teach or suggest all elements of claim 32.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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